Notice of References Cited	Application/Control No. 09/865,847	Applicant(s)/Patent Under Reexamination KAXIRAS ET AL.	
	Examiner Chun Cao	Art Unit 2115	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,510,494	01-2003	Arimilli et al.	711/137
	B	US-6,473,814	10-2002	Lyons et al.	710/35
	C	US-6,385,697	05-2002	Miyazaki, Mitsuhiro	711/128
	D	US-6,345,336	02-2002	Takahashi, Masafumi	711/125
	E	US-6,138,213	10-2000	McMinn, Brian D.	711/137
	F	US-6,157,977	12-2000	Sherlock et al.	710/310
	G	US-6,070,232	05-2000	Ishida et al.	711/143
	H	US-6,041,401	03-2000	Ramsey et al.	712/43
	I	US-5,835,949	11-1998	Quattromani et al.	711/135
	J	US-5,813,028	09-1998	Agarwala et al.	711/118
	K	US-5,813,022	09-1998	Ramsey et al.	711/3
	L	US-5,632,038	05-1997	Fuller, Samuel	713/324
	M	US-5,430,683	07-1995	Hardin et al.	365/227

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"Automatic Cache Line Access Monitoring" IBM TDB, Vol. 37, No. 6A, June 1994, page 299.
	V	K. Stein, et al., "Storage Array and Sense/Refresh Circuit for Single Transistor Memory Cells", IEEE Journal of Solid State Circuits, Vol. SC-7, No. 5, 336-340 (October 1972).
	W	K. Stein, et al., Session V: Memory II, "Storage Array and Sense/Refresh Circuit for Single Transistor Memory Cells", IEEE International of Solid State Circuits conference, 1972, pages 56-57.
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.